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MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Unit – I: Introduction to Embedded Systems

Unit – II: Microcontrollers and Processor Architecture & Interfacing
8051 Architecture, Input/Output Ports and Circuits, External Memory, Counters and Timers, PIC Controllers. Interfacing Processor (8051, PIC), Memory Interfacing, I/O Devices, Memory Controller and Memory arbitration Schemes.

Unit – III: Embedded RISC Processors & Embedded System-on-Chip Processor
PSOC (Programmable System-on-Chip) architectures, Continuous Timer blocks, Switched Capacitor blocks, I/O blocks, Digital blocks, Programming of PSOC, Embedded RISC Processor architecture – ARM Processor architecture, Register Set, Modes of operation and overview of Instructions

Unit – IV: Interrupts & Device Drivers
Exceptions and Interrupt handling Schemes – Context & Periods for Context Switching, Deadline & interrupt latency. Device driver using Interrupt Service Routine, Serial port Device Driver, Device drivers for Internal Programmable timing devices

Unit – V: Network Protocols
Serial communication protocols, Ethernet Protocol, SDMA, Channel & IDMA, External Bus Interface

TEXT BOOKS:


REFERENCES:

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

UNIT –I
Programmable logic: ROM, PLA, PAL PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD’s- CPLD (Mach 1to 5), Cypress FLASH 370 Device technology, Lattice PLST’s architectures – 3000 series – Speed performance and in system programmability.

UNIT – II
FPGAs: Field Programmable gate arrays- Logic blocks, routing architecture, design flow technology mapping jfor FPGAs, Case studies Xitrix XC4000 & ALTERA’s FLEX 8000/10000 FPGAs: AT &T ORCA’s (Optimized Reconfigurable Cell Array): ACTEL’s ACT-1,2,3 and their speed performance

UNIT-III
Alternative realization for state machine chat suing microprogramming linked state machine one –hot state machine, petrinetes for state machines-basic concepts, properties, extended petrinetes for parallel controllers.

UNIT-IV
Digital front end digital design tools for FPGAs& ASICs: Using mentor graphics EDA tool (“FPGA Advantage”) – Design flow using FPGAs

UNIT - V
Case studies of paraller adder cell paraller adder sequential circuits, counters, multiplexers, parellel controllers.

TEXT BOOKS:
2. Field Programmable Gate Arrays, John V.Oldfield, Richard C Dore, Wiley Publications.

REFERENCES :
UNIT – I:
Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology, Trends And Projections.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: \( I_{ds} - V_{ds} \) relationships, Threshold Voltage \( V_t \), \( G_m \), \( G_{ds} \) and \( \omega_o \), Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II:

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT – III:
COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT – IV:
SEQUENTIAL SYSTEMS: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT – V:
FLOOR PLANNING & ARCHITECTURE DESIGN: Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

TEXT BOOKS:

REFERENCES:
ALGORITHMS FOR VLSI DESIGN AUTOMATION

UNIT I
PRELIMINARIES
Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II
GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION
Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III
LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING
Problems, Concepts and Algorithms.

UNIT IV
MODELLING AND SIMULATION
Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT V
LOGIC SYNTHESIS AND VERIFICATION
Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

UNIT VI
HIGH-LEVEL SYNTHESIS

UNIT VII
PHYSICAL DESIGN AUTOMATION OF FPGA’S
FPGA technologies, Physical Design cycle for FPGA’s, partitioning and Routing for segmented and staggered Models.

UNIT VIII
PHYSICAL DESIGN AUTOMATION OF MCM’S

TEXT BOOKS:


REFERENCES:

HARDWARE- SOFTWARE CO-DESIGN
(ELECTIVE-I)

UNIT –I
CO-DESIGN ISSUES
Co-Design Models, Architectures, Languages, A Generic Co-design Methodology.

CO-SYNTHESIS ALGORITHMS:
Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II
PROTOTYPING AND EMULATION:
Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

TARGET ARCHITECTURES:
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT – III
COMPIALUTION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES:
Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT – IV
DESIGN SPECIFICATION AND VERIFICATION:
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT – V
LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I
System – level specification, design representation for system level synthesis, system level specification languages,

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II
Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS:
2. Hardware / software co- design Principles and Practice, 2002, kluwer academic publishers
DIGITAL SYSTEM DESIGN
(ELECTIVE-I)

Unit-I: Designing with Programmable Logic Devices

Unit-II: Fault Modeling & Test Pattern Generation

Unit-III: Fault Diagnosis in Sequential Circuits

Unit-IV: PLA Minimization and Testing
PLA Minimization – PLA folding, Fault model in PLA, Test generation and Testable PLA Design.

Unit-V: Minimization and Transformation of Sequential Machines

TEXT BOOKS:
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCES:
UNIT I:
**Introduction to Semiconductor Physics:** Review of Quantum Mechanics, Boltzman transport equation, continuity equation, Poisson equation

**Integrated Passive Devices:** Types and Structures of resistors and capacitors in monolithic technology, dependence of model parameters on structures

UNIT II:
**Integrated Diodes:** Junction and Schottky diodes in monolithic technologies – static and dynamic behavior – small and large signal models – SPICE models

**Integrated Bipolar Transistor:** Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model- dynamic model, parasitic effects – SPICE model – parameter extraction

UNIT III:
**Integrated MOS Transistor:** nMOS and pMOS transistor – threshold voltage – threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT IV:

UNIT V:
**Modeling of Hetero Junction Devices:** Band gap Engineering, Bandgap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar Transistors (HBTs), SiGe

**TEXT BOOKS:**

**REFERENCES:**
ADVANCED DIGITAL SIGNAL PROCESSING  
(ELECTIVE-II)

UNIT I  
Review of DFT, FFT, IIR Filters, FIR Filters,  
**Multirate Signal Processing:** Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion, Applications of Multirate Signal Processing

UNIT II  
**Non-Parametric methods of Power Spectral Estimation:** Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey methods, Comparison of all Non-Parametric methods

UNIT III  

UNIT –IV  
**Linear Prediction** : Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

UNIT V  
**Finite Word Length Effects:** Analysis of finite word length effects in Fixed-point DSP systems – Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality – Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXTBOOKS:

2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.  

REFERENCES:

2. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education  
UNIT-I
Introduction:

UNIT-II
Modern Techniques:
Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

UNIT-III
Conventional Encryption
Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.
Public Key Cryptography
Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT-IV
Number theory
Prime and Relatively prime numbers, Modular arithmetic, Fermat’s and Euler’s theorems, Testing for primality, Euclid’s Algorithm, the Chinese remainder theorem, Discrete logarithms.
Message authentication and Hash functions:
Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT-V
Hash and Mac Algorithms
MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. Digital signatures and Authentication protocols:
Digital signatures, Authentication Protocols, Digital signature standards.

UNIT-VI
Authentication Applications:

UNIT-VII
IP Security
Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.
Web Security

UNIT-VIII
Intruders, Viruses and Worms: Intruders, Viruses and Related threats.
Fire Walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

REFERENCES:
1. Principles of Network and Systems Administration, Mark Burgess, John Wiel
UNIT –I
Introduction, basic structures of MEM devices – (Canti-Levers, Fixed Beams diaphragms). Broad Response of Micro electromechanical systems (MEMS) to Mechanical (Force, pressure etc.) Thermal, Electrical, optical and magnetic stimuli, compatibility of MEMS from the point of power dissipation, leakage etc.

UNIT –II

UNIT – III
Two terminal MEMS - capacitance Vs voltage Curve – variable capacitor. Applications of variable capacitors. Two terminal MEM structures.
Three terminal MEM structures – controlled variable capacitors – MEM as a switch and possible applications.

UNIT – IV
MEM circuits & structures for simple GATES- AND, OR, NAND, NOR, Exclusive OR<simple MEM configurations for flip-flops triggering applications to counters, converters. Applications for analog circuits like frequency converters, wave shaping. RF Switches for modulation. MEM Transducers for pressure, force temperature. Optical MEMS.

UNIT – V
MEM Technologies: Silicon based MEMS- process flow – brief account of various processes and layers like fixed layer, moving layers spacers etc., and etching technologies.

TEXT BOOKS:

REFERENCES:
SIMULATION LAB (VLSI)

CYCLE 1:

1. Digital Circuits Description using Verilog.
2. Verification of the functionality of designed Circuits using function simulator.
3. Timing Simulation for critical Path time calculation.
5. Place and route techniques for major FPGA Vendors using Xilinx, Altera, Cypress etc.,

CYCLE 2:

2. NMOS, PMOS Characteristics.
3. Layout basics- INV, NAND, NOR, EXOR, EXNOR.
4. Layout of adder, subtractor, multiplexer.
5. Layout Comparator.

For Experiments in cycle 2: 3,4,5: Draw the Schematics Perform Simulation, Extract the Layout, Run Physical Verification (DRC, LVS, PEX) and post layout simulation.