II B.Tech II Semester Examinations, December-January, 2011-2012
SWITCHING THEORY AND LOGIC DESIGN
Common to Bio-Medical Engineering, Electronics And Telematics,
Electronics And Communication Engineering, Electrical And Electronics
Engineering

Time: 3 hours Max Marks: 75

Answer any FIVE Questions
All Questions carry equal marks

1. (a) What are Self complementing codes? Give examples.
   (b) Write the procedure for constructing Hamming codes. Construct hamming
codes for the decimal numbers 1,4,8. [8+7]

2. Design a combinational circuit whose input is a 3 input binary number and whose
output is a 2’s complement of the input number. [15]

3. Implement the following functions using Multiplexer
   \[ F_1 = \Sigma m(2,3,6,8,12) \]
   \[ F_2 = \Sigma m(1,3,5,6,7,8,10) \]
   \[ F_3 = \Sigma m(1,3,4,5,6,13,14) \]
   \[ F_4 = \Sigma m(2,3,4,8,9,11,14) \] [15]

4. (a) Design a clocked SR flip flop. Explain its operation with the help of charac-
teristic table and characteristic equation. Give the symbol of edge triggered
SR flipflop.
   (b) Explain the operation of JK flipflop with the help of input output waveforms.
   [8+7]

5. Minimize the following incompletely specified machine using Merger Graph method.
   [15]

<table>
<thead>
<tr>
<th>PS</th>
<th>NS,Z</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I1</td>
</tr>
<tr>
<td>A</td>
<td>-</td>
</tr>
<tr>
<td>B</td>
<td>E,0</td>
</tr>
<tr>
<td>C</td>
<td>F,0</td>
</tr>
<tr>
<td>D</td>
<td>-</td>
</tr>
<tr>
<td>E</td>
<td>-</td>
</tr>
<tr>
<td>F</td>
<td>C,0</td>
</tr>
</tbody>
</table>


7. Use De Morgan’s rules to show that
   (a) A NOR gate with inverted inputs acts like an AND gate.
   (b) A NAND gate with inverted inputs acts like an OR gate
(c) An AND gate with inverted inputs acts like a NOR gate.

(d) \((X+Y)(X+YZ)+X'Y' +X'Z' = 1\) \[15\]

8. Design a synchronous sequential circuit which converts a binary number into a BCD number. Design the ASM chart to implement the above mentioned design. Design the Data processing unit and the control unit using PLA control. \[15\]

★★★★★
1. Explain the following Huntington’s Postulates with suitable examples
   (a) Commutative Law
   (b) Distributive Law
   (c) Intersection Law
   (d) Complements Law

2. (a) Design a 3 bit Ring counter. Discuss how Ring counters differ from Twisted Ring counter.
   (b) Give the design steps of asynchronous counters. Design a Mod-5 counter to count the sequence 1, 3, 5, 6, 7, 1. Use D flip flops.

3. (a) Draw the block diagram of a ROM. Define address and word. Relate the number of output lines with number of bits in a word. How an output word can be selected?
   (b) For a 64 x 8 ROM, determine the number of words it contains and the size of each word. How many output lines are there for the ROM?

4. (a) Use 1’s complement arithmetic to subtract
   i. (54)\textsubscript{10} from (231)\textsubscript{10}
   ii. (-27)\textsubscript{10} - (87)\textsubscript{10}
   (b) Determine the largest and smallest Hexadecimal numbers that can be used in a 16-bit digital system.

5. (a) State and explain with examples the state equivalence and distinguishable theorems.
   (b) Give the procedure to find the compatibility graph and minimal cover table.

6. (a) Write the procedure to convert sum of product form to product of sum form
   (b) Use a Karnaugh map to convert F =\overline{A}\overline{B} + \overline{A}\overline{B} + \overline{A}B\overline{C} + \overline{A}\overline{B} into its POS form.
7. Draw an ASM chart for the state table given below. Design a control unit with the help of D-Flip flop and decoders. [15]

<table>
<thead>
<tr>
<th>PS</th>
<th>NS</th>
<th>X = 0</th>
<th>X = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>011,0</td>
<td>100,1</td>
<td></td>
</tr>
<tr>
<td>001</td>
<td>001,0</td>
<td>100,1</td>
<td></td>
</tr>
<tr>
<td>010</td>
<td>010,0</td>
<td>000,1</td>
<td></td>
</tr>
<tr>
<td>011</td>
<td>001,0</td>
<td>010,1</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>010,0</td>
<td>011,0</td>
<td></td>
</tr>
</tbody>
</table>

8. (a) Design a multiple output combinational logic network which subtracts two bits of binary data producing a different bit D and a borrow bit B as two output signals.

(b) Design a Magnitude comparator to compare two 3 bit numbers. [8+7]
1. A receiver has received a message code 1110110 which is an even parity Hamming code. Determine whether the message code has any error. If so correct the error. Give proper reasoning for your answer. [15]

2. Express the following in standard SOP form
   
   (a) \( F = (A+B+C')(A+B')(B+C') \)
   
   (b) \( F = (X+Y'+Z)(X'+Y+Z')(W+X+Y') \)
   
   (c) \( F = (P'+Q+R+S')(R'+S)(Q'+R+S) \)
   
   (d) \( F = (M'NP)+(MNP')+(NP') \) [15]

3. (a) Define the following terms
   
   i. Boolean function
   
   ii. Sum of products form
   
   iii. Product of sum form
   
   iv. Don’t care conditions
   
   (b) Convert the following expressions into their respective canonical forms:
   
   i. \( WY + W'XZ + WYZ' \)
   
   ii. \( (W + X + Y')(W + Z) \) [8+7]

4. Implement the following Boolean function using PROM
   
   (a) \( F1(A,B,C,D) = \Sigma m(1,3,5,7,9,11) \)
   
   (b) \( F2(A,B,C,D) = \Sigma m (0,2,4,6,9) \) [15]

5. (a) Design a logic circuit which converts serial input to parallel output.

   (b) Design a combinational logic circuit which compares two 4 bit numbers \( A \& B \) and produces 3 outputs to indicate whether \( A > B \) or \( A = B \) or \( A < B \). [8+7]

6. Find the equivalence partition for the machine shown in figure. Show a standard form of the corresponding reduced machine. Find a minimum length sequence that distinguishes state A from state B. [15]
7. Obtain the ASM charts for the following state transition

(a) If $Q = 0$, control goes from G1 to state G2, If $Q = 1$, generate the conditional operation and go from G1 to G2.

(b) If $Q = 1$, control goes from G1 to G2 and then to G3, if $Q = 0$, control goes from G1 to G3.

(c) Start from the state G1, then if $QR = 00$, go to G2, if $QR = 01$, then go to G3, if $QR = 10$, then go to G1, otherwise go to G3 and design its control circuit using D flip flop and decoder. [15]

8. Design a 4 bit counter that counts either in Binary or gray depending on the input given to the select line. When select line = 0, the counter is to count in Binary, and when select line = 1, the counter is to count in gray. Draw the logic diagram. [15]
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1. (a) Encode each of the 10 decimal digits 0,1,2,3,4,5,6,7,8,9 by means of gray codes.
(b) Write short notes on Hexa decimal codes and alpha numeric codes with suit-
able examples. [8+7]

2. (a) How Programmable Logic array is advantageous over ROMs? What is meant
by an LSI device?
(b) Give the block diagram of PLA. Which are the terms are programmable? How
inverter is useful in the PLA construction at the output? [8+7]

3. Explain the construction and working of SR flip Flop for different input conditions.
Explain in detail the output conditions of SR flip flop if S=R=1. How the circuit is
modified to avoid this conditions. [15]

4. (a) Define the function of a decoder. Design a 3 to 8 decoder. Draw the circuit
diagram, function table and explain the working of the decoder circuit.
(b) Design a BCD to Decimal decoder. [8+7]

5. Write the procedure to obtain a multilevel NAND circuit from a given Boolean
function. Consider the following Boolean function to demonstrate the procedure.
\[ F = [(AC' + B'D).(BC' + AD)]E' + (CF' + DG) \] [15]

6. (a) Draw the State diagram of a sequence detector which is designed to detect
the pattern 1011 in the input sequence. Draw the ASM chart for the state
diagram. Explain the sequence of operations of each block.
(b) Discuss with the help of an example, in an ASM block, all the operations that
are performed within the block must occur in synchronism during the edge
transition of the same clock pulse while the system changes from one state to
the next state. [8+7]

7. Design a combinational logic circuit that has 3 inputs. The output is required to
go HIGH whenever the number of inputs have even number of 1’s. Draw the Truth

8. An unknown 2 input, three state machine produces the output sequence Z in re-
sponse to the input sequence X:
X = 0 1 0 0 1 0 1 0 0 0 1 0
Z = 1 0 1 1 0 1 1 1 0 0 0 1

Assuming that A is the initial state, determine the reduced standard form description of the machine.